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10/038,546	10/24/2001	Alexander I. Krymski	08305-118001	7123

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EXAMINER	
QUIETT, CARRAMAH J	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,546	KRYMSKI, ALEXANDER I.	
	Examiner	Art Unit	
	Carramah J. Quiett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 12-16, and 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Miura (U.S. #6,501,506).

As for claim 1, Miura discloses a circuit diagram in the seventh mode of implementation of his solid state pick-up unit. As shown in figure 16, the circuit comprises: a pixel including (i) a buffer transistor (ref. 8) having an input, (ii) first (ref. 12b) and second (ref. 12a) capacitive storage elements each of which selectively can be coupled to the input of the buffer transistor via transfer transistors 10b and 10a, respectively, and (iii) a photosensitive element (ref. 2) having an output which selectively can be coupled to the input of the buffer transistor via transfer transistor 4; and a readout circuit (refs. 60, 72, 52) that selectively can be coupled to an output of the buffer transistor (col. 11, lines 8-14 and 30-36). Also, please read column 1, lines 21-28.

For claim 2, Miura's circuit of claim 1 including: a first switch (ref. 4) coupled between the output of the photosensitive element and the input of the buffer transistor; a second switch (ref. 10b) coupled between the first capacitive storage element and the input of the buffer transistor', and a third switch (ref. 10a) coupled between the second capacitive storage element

and the input of the buffer transistor, each of the switches being selectively operable in an open or closed state. Also, please read column 10, lines 66-67 and column 11, lines 1-13.

As for claim 3, Miura's circuit of claim 2 including a fourth switch (fig. 16, ref. 6) coupled between a power supply node and the input of the buffer transistor, the fourth switch being selectively operable in an open or closed state. Also in figure 16, the fourth switch (ref. 6) is connected to a power supply node via potential of wire 42. In fact, the fourth switch can be turned on (closed) (col. 11, lines 17-18). Therefore, it can be turned off (opened) as well.

As for claim 4, Miura's circuit of claim 3 including a controller for providing signals to control the respective states of the first, second, third and fourth switches. In figure 16, Miura illustrates control lines 92, 96, and 98 from the vertical shift register (ref. 60) for controlling the fourth (ref. 6), second (ref. 10b), and third (10a) switches, respectively (col. 10, line 66-67; col. 11, lines 1-13). The first switch (ref. 4) is controlled by a TRANSFER signal, which turns it on or off (col. 11, lines 60-64).

As for claim 12, Miura's prior art circuit of claim 3 wherein the fourth switch is configured for operation in a sub-threshold reset mode. As stated in Miura's disclosure and illustrated in figure 16, the reset transistor (ref. 6) and the sample hold transistors (refs. 10a, 10b) are turned on and the potential of the wiring 42 is set low (col. 11, lines17-19) as well as adjusting the variation in the threshold value (col. 11, 45-46).

As for claim 13, Miura discloses a circuit in the seventh mode of implementation of his solid state pick-up unit comprising: an array of pixels, in figure 16, each of which is associated with a respective row and column in the array, each pixel, as shown in figure 1, including (i) a buffer transistor (ref. 8) having an input, (ii) first (ref. 12b) and second (ref. 12a) capacitive

storage elements each of which selectively can be coupled to the input of the buffer transistor via transfer transistors 10a and 10b, respectively, and (iii) a photosensitive element (ref. 2) having an output which selectively can be coupled to the input of the buffer transistor via transfer transistor 4; readout circuitry (refs. 60, 72, 52) which selectively can be coupled to outputs of buffer transistors of selected pixels in the array (col. 11, lines 8-14 and 30-36); and a controller for providing signals to control the selective coupling of the first (ref. 12b) and second (ref. 12a) capacitive storage elements and the photosensitive element (ref. 2) to the input of the buffer (ref. 8) and to control the selective coupling of the readout circuitry to the outputs of the buffer transistors. In figure 16, Miura illustrates control lines 96 and 98 from the vertical shift register (ref. 60) for controlling the first (ref. 12b) and second (ref. 12a) capacitive storage elements via the second (ref. 10b), and third (ref. 10a) switches, respectively (col. 11, lines 8-13). Additionally, the photosensitive element (ref. 2) to the input of the buffer (ref. 8) is controlled by a TRANSFER signal via the fourth switch (ref. 4), which turns it on or off (col. 11, lines 60-64).

Claims 14-16 and 24 are integrated circuit claims and are written similar for claims 2-5 and 12. Please read the rejections for claims 2-5 and 12 for the reasons for rejecting claims 14-16 and 24, respectively.

Claim 25 is a method claim and is written similar to claim 1. Please read the rejection for claim 1 for the reason for rejecting claim 25.

As for claim 26, Miura discloses the method of claim 25 including obtaining a signal representing the difference between the first and second signal levels read from the pixel in column 11, lines 30-36.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-11, 17-23, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura in view of Numazaki et al. (U.S. #6,628, 335).

As for claim 5, Miura discloses a circuit of claim 4 wherein the controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element and to cause the second capacitive element to store a second signal level sensed by the photosensitive element. Please read column 11, lines 17-36. However, he does not explicitly disclose a circuit of claim 4 wherein the controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time.

Nevertheless, Numazaki teaches an image capturing apparatus (col. 3, lines 41-43) where the timing controller (fig. 1, ref. 9) controls the operation of the image detecting section (fig. 1, ref. 4). The cell (ref. 15) of image detecting section, illustrated in figure 2, comprises an accumulation control section (ref. 11) that controls where the image signal of the photo-electric converter section should be accumulated. Signals are accumulated in the first and second charge accumulating sections (refs. 12 and 13). This means that the timing controller is configured for

providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time. Please read column 1, lines 26-37 and column 3, lines 45-66.

Furthermore, in Miura's disclosure, charges are stored in the first and second capacitive elements (fig. 16, ref. 12b and 12a, respectively) connected in parallel and subsequently read out two times. Miura also states that the timing of the signal storage period can be generated by an externally provided timing circuit and by timing the reading by an internally provided timing circuit. Please read column 12, lines 30-35. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the limitations of claim 5 with the image pick-up device of Miura in order to provide an image capture module for inputting a shape of an object on a three-dimensional space (Numazaki, col. 1, lines 45-47).

As for claim 6, Miura teaches a circuit of claim 5 wherein the controller is configured for providing signals to cause (i) the first and second switches to be closed during the first integration time, (ii) the third and fourth switches to be open during the first integration time, (iii) the first and third switches to be closed during the second integration time, and (iv) the second and fourth switches to be open during the second integration time. Referring to the figure 16 of Miura, please note that Examiner considers the first switch to be reference # 4, the second switch to be reference #10b, the third switch to be reference #10a, and the fourth switch to be reference #6. Please read column 10, line 66-67 and column 11, lines 1-13 and lines 60-64. Miura teaches that after the potential of the wiring is returned to its original high potential, the charges are injected into the first and second sample and hold capacitors. According to the structure of the

circuit diagram illustrated in figure 16, it is inherent for the first and second switches to be on during the first integration time, the third and fourth switches to be off during the first integration time, so that the charges can be injected into only the first capacitor without resetting. Similarly, it is also inherent, according to the structure of the circuit diagram in figure 16, for the first and third switches to be on during the second integration time and the second and fourth switches to be off during the second integration time, so that the charges can be injected into only the second capacitor without resetting. Lastly, claim 6 is dependent on claim 5. Please refer to the rejection for claim 5 for the reasons for obviousness.

As for claim 7, Miura teaches a circuit of claim 6 wherein the controller is configured for providing signals to cause (i) the first, second and fourth switches to be closed just prior to the first integration period, and (ii) the first, third and fourth switches to be closed just prior to the second integration period. Referring to the figure 16 of Miura, please note that Examiner considers the first switch to be reference # 4, the second switch to be reference #10b, the third switch to be reference #10a, and the fourth switch to be reference #6. Please read column 10, line 66-67 and column 11, lines 1-13 and lines 60-64. According to the structure of the circuit diagram illustrated in figure 16, it is inherent for Miura's circuit to perform the limitations listed above so that only one storage capacitor can reset one at a time and so that the charging process can be complete before the next one begins. Please refer to the rejection for claim 6 for the reasons for obviousness.

As for claim 8, Miura's circuit of claim 6 wherein the controller is configured for providing capacitive storage element prior to the second integration period signals to reset the photosensitive element and the first capacitive storage element prior to the first integration

period and to reset the photosensitive element and the second. Referring to the figure 16 of Miura, please note that Examiner considers the first switch to be reference # 4, the second switch to be reference #10b, the third switch to be reference #10a, and the fourth switch to be reference #6. Please read column 10, line 66-67 and column 11, lines 1-13 and lines 60-64. According to the structure of the circuit diagram illustrated in figure 16, it is inherent for Miura's circuit to perform the limitations listed above so that the charging process can be complete before the next one begins. Please refer to the rejection for claim 6 for the reasons for obviousness.

As for claim 9, Miura discloses a circuit wherein the controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element and to cause the second capacitive element to store a second signal level sensed by the photosensitive element. Please read column 11, lines 17-36. However, Miura does not explicitly disclose a controller configured for providing signals to selectively transfer the first signal level from the first capacitive storage element to the readout circuit and to transfer the second signal level from the second capacitive storage element to the readout circuit. His disclosure states that the corresponding components of his circuit are selected for signal charges to be stored in the first and second storage capacitors.

Numazaki discloses an image capturing apparatus (col. 3, lines 41-43) a timing controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time. Please read column 1, lines 26-37 and column 3, lines 45-66. His timing controller is further configured for providing signals to selectively transfer the first

signal level from the first capacitive storage element to the readout circuit and to transfer the second signal level from the second capacitive storage element to the readout circuit. His disclosure states that the corresponding components of his circuit are selected for signal charges to be stored in the first and second storage capacitors. Numazaki has an output section that selects either the fist charge accumulating section or the second charge accumulating section and reads its electric charge to the outside of the cell. Please read column 3, lines 59-67 and column 4, lines 1-2.

Furthermore, in Miura's disclosure, charges are stored in the first and second capacitive elements (fig. 16, ref. 12b and 12a, respectively) connected in parallel and subsequently read out two times. Miura also states that the timing of the signal storage period can be generated by an externally provided timing circuit and by timing the reading by an internally provided timing circuit. Please read column 12, lines 30-35. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the limitations of claim 9 with the image pick-up device of Miura in order to provide an image capture module for inputting a shape of an object on a three-dimensional space (Numazaki, col. 1, lines 45-47).

As for claim 10, Miura's circuit of claim 9 wherein the controller is configured for providing signals to reset the input of the buffer transistor (fig. 16, ref. 8) prior to transferring the first signal level from the first capacitive storage element (fig. 16, 10b) to the readout circuit and to reset the input of the buffer transistor prior to transferring the second signal level from the second capacitive storage element (fig. 16, 10a) to the readout circuit. According to the structure of the circuit diagram illustrated in figure 16, it is inherent for Miura's circuit to perform the

limitations listed above so that the charging process can be complete before the next one begins. Please refer to the rejection for claim 9 for the reasons for obviousness.

As for claim 11, Miura's prior art circuit of claim 9 wherein the controller is configured for providing signals to cause the fourth switch to be closed prior to transferring the first signal level from the first capacitive storage element to the readout circuit and to cause the fourth switch to be closed just prior to transferring the second signal level from the second capacitive storage element to the readout circuit. According to the structure of the circuit diagram illustrated in figure 16, it is inherent for Miura's circuit to perform the limitations listed above so that the charging process can be complete before the next one begins. Please refer to the rejection for claim 9 for the reasons for obviousness.

Claims 17-23 are an integrated circuit claims and is written similar for claims 5-11, respectively. Please read the rejection for claims 5-11 for the reasons for rejecting claims 17-23, respectively.

As for claim 27, Miura discloses the method of claim 25 wherein the first signal level is stored and the second signal level is stored. Miura's disclosure reveals that there are first (ref. 12a) and second (ref. 12a) capacitive storage elements in the circuit. Please read column 11, lines 30-36. However, Miura does not disclose a the method of claim 25 wherein the first signal level is stored during a first integration period and the second signal level is stored during a second integration period.

On the other hand, Numazaki teaches an image capturing apparatus (col. 3, lines 41-43) where the timing controller (fig. 1, ref. 9) controls the operation of the image detecting section (fig. 1, ref. 4). The cell (ref. 15) of image detecting section, illustrated in figure 2, comprises an

accumulation control section (ref. 11) that controls where the image signal of the photo-electric converter section should be accumulated. Signals are accumulated in the first and second charge accumulating sections (refs. 12 and 13). This means that the timing controller is configured for providing signals cause the first signal level to be stored during a first integration period and the second signal level to be stored during a second integration period. Please read column 1, lines 26-37 and column 3, lines 45-66.

Furthermore, in Miura's disclosure, charges are stored in the first and second capacitive elements (fig. 16, ref. 12a and 12b, respectively) connected in parallel and subsequently read out two times. Miura also states that the timing of the signal storage period can be generated by an externally provided timing circuit and by timing the reading by an internally provided timing circuit. Please read column 12, lines 30-35. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the limitations of claim 27 with the image pick-up device of Miura in order to provide an image capture module for inputting a shape of an object on a three-dimensional space (col. 1, lines 45-47).

Claim 28 is a method claim dependent on claim 27 and is written similar to claim 8. Please read the rejection for claim 8 for the reason for rejecting claim 28.

Claim 29 is a method claim dependent on claim 28 and is written similar to claim 10. Please read the rejection for claim 10 for the reason for rejecting claim 29.

As for claim 30, Miura discloses a method of claim 28 including operating a pixel reset switch in a sub-threshold reset mode. As stated in Miura's disclosure and illustrated in figure 16, the reset transistor (ref. 6) and the sample hold transistors (refs. 10a, 10b) are turned on and the potential of the wiring 42 is set low (col. 11, lines17-19) as well as adjusting the variation in the

threshold value (col. 11, 45-46). Furthermore, claim 30 is dependent on claim 28. Please read the rejection for claim 28 for the reasons for obviousness in view of Numazaki et al.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patents			
6,628,335	Beiley	6,384,394	Afghahi
6721007	Tani et al.	6,720,592	Kindt et al.
6,078,037	Booth	5,438,365	Yamashita et al.
6,522,357	Beiley	6,246,436	Lin et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (703) 305-0566. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.J.Q.
Oct. 29, 2004

NGOC YEN VU
PRIMARY EXAMINER